REMARKS

I.   Introduction

Claims 1, 3-10 and 12 are currently pending. Reconsideration of the patentability of the pending claims is respectfully requested In view of the following remarks.

II.   Rejection of Claims 1, 3-8, 10 and 12 under 35 U.S.C. § 103(a)

Claims 1, 3-8, 10 and 12 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Whetsel, U.S. Patent 6,408,413 ("Whetsel").

In rejecting a claim under 35 U.S.C. § 103(a), the Examiner bears the initial burden of presenting a prima facie case of obviousness. In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). To establish prima facie obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974).

Independent claim 1 recites a method for activating a microprocessor arranged as a part of a microcontroller within a framework of a boundary scan test procedure using a JTAG interface of the microprocessor that includes steps of: i) activating the JTAG interface of the microprocessor with a test routine that is executable on the microprocessor; and ii) transmitting a test data stream provided by the test routine to the JTAG interface from the microprocessor, wherein I/O ports of the microprocessor are connected to pins of the JTAG interface, and a data-in pin of

the JTAG interface is activated using the test routine via the I/O ports.

Regarding claim 1, and the subject matter of the present invention in general, the specification clearly explains that a main purpose of the invention is to enable the testing of a microcontroller even when a JTAG interface is not externally accessible. (See Specification, page 3, lines 19-21). The Whetsel reference does not disclose or suggest these features of claim 1; instead, Whetsel unambiguously refers to "an architecture wherein all TAPS [test access ports] of an IC can be controlled and accessed from an external 1149/1 test bus *via a single externally accessible 1149.1 TAP interface*." (Whetsel, col. 2, lines 55-58 (emphasis added)). Figure 2 of Whetsel, which is referred to as an "exemplary IC according to the invention," depicts an externally accessible interface 20 including TDI[test data in], TCK, TMS, TRST* and TDO [test data out] pins. (Whetsel, col. 4, lines 15-20). The crucial fact to note here is that the test data-in (TDI) pin of the interface 20 ultimately receives data *from an external source,* and the test data-out (TDO) pin ultimately provides data to an external sink.

While the Examiner contends that I/O ports TD1, TD01-TD04 of the IC core circuitry of Whetsel are connected to the TDI and TDO pins of the JTAG interface, and that the TDI pin of the JTAG interface is activated using a test routine via the I/O ports, it is unclear how this can be the case. As shown in Figure 2 of Whetsel, none of the outputs of the TAPs (TD01, TD02, TD03, TD04) or the output of the TAP linking module (25) are linked to TDI; rather, they are coupled to an IC output pin TDO (27) via a "3S MUX." Thus, it is apparent that the IC (10) does not provide data to the TDI pin and, therefore, the IC does not provide the test routine data itself. To the contrary, Whetsel (unlike the Applicants' claimed subject matter) is not directed to providing an internal test JTAG test procedure for an inaccessible IC, but rather, is directed to selectively enabling one of the TAPs to be accessed via the IC's 1149.1 test pins. (Whetsel, col. 4, lines 46-48).

For at least these reasons, it is submitted that Whetsel clearly does not solve the problem that the present invention addresses and, in particular, Whetsel does not disclose or suggest the features of claim 1, or the features of its dependent claims 3 to 8. Since independent claim 10 recites features analogous to those of claim 1, it is submitted that Whetsel also does not disclose or suggest the features of claim 10, or the features of its dependent claim 12. Withdrawal of the obviousness rejection of claims 1, 3-8, 10 and 12 is therefore respectfully requested.

III. Rejection of Claim 9 under 35 U.S.C. § 103(a)

Claim 9 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Whetsel in view of U.S. Patent 5,357,432 to Margolis et al. ("Margolis").

Claim 9 depends from, and incorporates the limitations of, claim 1. The Margolis reference merely refers to an automatic guidance control system that includes a microcontroller. Since Margolis does not in any way refer to a boundary scan procedure according to IEEE 1149, let alone refer to specific ways of implementing such a procedure, Margolis fails to cure the critical deficiencies of the primary Whetsel reference discussed above with respect to claim 1. Therefore, the combination of Whetsel and Margolis references does not disclose or suggest all features of claim 1, from which claim 9 depends. For at least these reasons, claim 9 is not rendered obvious by Whetsel and Margolis.

Withdrawal of the obviousness rejection of claim 9 is therefore respectfully requested.
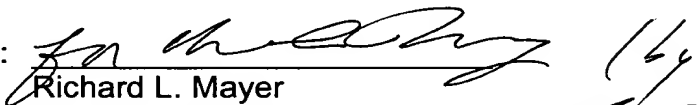
CONCLUSION

In light of the foregoing, Applicants respectfully submit that all of the pending claims are in condition for allowance. Prompt reconsideration and allowance of the present application are therefore earnestly solicited.

Respectfully submitted,

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